

## EAST SEARCH

9/19/05

L#	Hits	Search String	Databases
L1	49	dual threshold voltage	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	432622	(integrated or digital) adj circuit\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	72	((integrated or digital) adj circuit\$1) and (dominant near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	256	((integrated or digital) adj circuit\$1) and (partial near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	0	3 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	43	dominant logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	19	2 and 6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	17	3 and (determin\$3 with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	4	3 and (determin\$3 with dominant with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	25	4 and (determin\$3 with partial with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	3	10 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	84	2 and (partial same (logic near2 state))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	30	4 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	0	12 and 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	4	2 and (partial near2 logic near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	15	2 and (partial with "logic state")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	3	2 and ("partial logic" with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	0	2 and ("partial logic state")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	15960	((integrated or digital) adj circuit\$1) and (leakage near2 current\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	280	19 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	11	12 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	68	20 and (logic near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	1	22 and (partition\$1 same(logic near2 state))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	5	circuit design and "dual threshold voltage"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	1358	(dual or two or multiple) near2 "threshold voltage"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	40	25 and "circuit design" and (leakage near2 current\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	2	determin\$3 with "dominant state" with logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	93	25 and "circuit design"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	4	dominant logic state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	20	dominant state with logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	16	logic state with dominant	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	50	2 and (partition\$1 with "power supply")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	5	DC-connected component or "DC connected component" or "DC-connected comp	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L34	0	2 and "cone of influence"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

L35	0	2 and "cone of transistors"			USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	462202	(integrated or digital) adj circuit\$1			USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	47	1 and ("logic state" with "leakage current")			USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	16818	703/\$.ccls. or "716"/\$.ccls.			US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L3	0	2 and "dominant logic state"			US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L4	6	2 and "dominant logic"			US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L5	1	2 and "dominant logic".CLM.			US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L6	5	dominant logic.CLM.C151			US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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### Results of search set L33:(dual or two or multiple) near2 "threshold voltage" ) and "circuit design"

Document Kind	Codes	Title	Issue Date	Current OR	Abstract
US	20030170938 A1	Thin film semiconductor device and method for manufacturing same	20030911	438/166	
US	20030071315 A1	Reprogrammable non-volatile memory using a breakdown phenomena in an ultra-	20030417	257/390	
US	20030071296 A1	Reprogrammable non-volatile memory using a breakdown phenomena in an ultra-	20030417	257/298	
US	20030070147 A1	Dual threshold gate array or standard cell power saving library circuits	20030410	716/2	
US	20030006816 A1	Semiconductor integrated circuit device and microcomputer	20030109	327/158	
US	20020177279 A1	Method for making multiple threshold voltage fet using multiple work-function gate	20021128	438/289	
US	20020175712 A1	CMOS skewed static logic and method of synthesis	20021128	326/98	
US	20020175643 A1	DUAL SIDED SELF-OSCILLATION CIRCUIT FOR DRIVING AN OSCILLATORY /	20021128	318/114	
US	20020154545 A1	Non-volatile memory device with plurality of threshold voltage distributions	20021024	365/185.22	
US	20020145174 A1	SOI FET and method for creating FET body connections with high-quality matching;	20021010	257/510	
US	20020093064 A1	Semiconductor device and method of fabricating the same	20020718	257/408	
US	20020030521 A1	Semiconductor integrated circuit device and microcomputer	20020314	327/158	
US	20010022753 A1	Circuit and method for timing multi-level non-volatile memories	20010920	365/203	
US	6615229 B1	Dual threshold voltage complementary pass-transistor logic implementation of a lo	20030902	708/629	
US	6608509 B1	Semiconductor integrated circuit device and microcomputer	20030819	327/149	
US	6597220 B2	Semiconductor integrated circuit device and microcomputer	20030722	327/158	
US	6593799 B2	Circuit including forward body bias from supply voltage and ground nodes	20030715	327/534	
US	6574146 B2	Circuit and method for timing multi-level non-volatile memories	20030603	365/185.2	
US	6548971 B2	Dual sided self-oscillation circuit for driving an oscillatory actuator	20030415	318/114	
US	6519184 B2	Non-volatile memory device with plurality of threshold voltage distributions	20030211	365/185.22	

US 6512274 B1	CMOS-process compatible, tunable NDR (negative differential resistance) device	20030128 257/369
US 6495891 B1	Transistor having impurity concentration distribution capable of improving short channel effect	20021217 257/404
US 6472916 B2	Semiconductor integrated circuit device and microcomputer	20021029 327/158
US 6448590 B1	Multiple threshold voltage FET using multiple work-function gate materials	20020910 257/202
US 6405348 B1	Deep sub-micron static timing analysis in the presence of crosstalk	20020611 716/4
US 6388483 B1	Semiconductor integrated circuit device and microcomputer	20020514 327/158
US 6373753 B1	Memory array having selected word lines driven to an internally-generated booster voltage	20020416 365/189.09
US 6363029 B1	Semiconductor device incorporating internal power supply for compensating for device variations	20020326 365/230.06
US 6348713 B1	Method for fabricating semiconductor device	20020219 257/347
US 6313511 B1	Semiconductor device	20011106 257/392
US 6300819 B1	Circuit including forward body bias from supply voltage and ground nodes	20011009 327/534
US 6232827 B1	Transistors providing desired threshold voltage and reduced short channel effects	20010515 327/537
US 6218895 B1	Multiple well transistor circuits having forward body bias	20010417 327/566
US 6208575 B1	Dynamic memory array bit line sense amplifier enabled to drive toward, but stoppage of, a threshold voltage	20010327 365/208
US 6198314 B1	Sample and hold circuit and method therefor	20010306 327/94
US 6198308 B1	Circuit for dynamic switching of a buffer threshold	20010306 326/83
US 6184746 B1	PLL power supply filter (with pump) having a wide voltage range and immunity to clock jitter	20010206 327/551
US 6169419 B1	Method and apparatus for reducing standby leakage current using a transistor structure	20010102 326/58
US 6166584 A	Forward biased MOS circuits	20001226 327/534
US 6166577 A	Semiconductor integrated circuit device and microcomputer	20001226 327/278
US 6161213 A	System for providing an integrated circuit with a unique identification	20001212 716/4
US 6128224 A	Method and apparatus for writing an erasable non-volatile memory	20001003 365/185.18
US 6125050 A	Configuration for driving parallel lines in a memory cell configuration	20000926 365/51
US 6100751 A	Forward body biased field effect transistor providing decoupling capacitance	20000808 327/534
US 6075727 A	Method and apparatus for writing an erasable non-volatile memory	20000613 365/185.22
US 6073208 A	Apparatus and method for reducing programming cycles for multistate memory systems	20000606 711/103
US 6014327 A	Memory apparatus including programmable non-volatile multi-bit memory cell, and method of programming	20000111 365/185.03
US 6014044 A	Voltage comparator with floating gate MOS transistor	20000111 327/81
US 5912571 A	Using the internal supply voltage ramp rate to prevent premature enabling of a device	19990615 327/143
US 5907855 A	Apparatus and method for reducing programming cycles for multistate memory systems	19990525 711/103
US 5831451 A	Dynamic logic circuits using transistors having differing threshold voltages	19981103 326/93
US 5821778 A	Using cascode transistors having low threshold voltages	19981013 326/95
US 5815446 A	Potential generation circuit	19980929 365/189.09
US 5815005 A	Power reduction circuits and systems for dynamic logic gates	19980929 326/95
US 5793698 A	Semiconductor read-only VLSI memory	19980811 365/230.08
US 5774367 A	Method of selecting device threshold voltages for high speed and low power	19980630 716/2
US 5757055 A	Triple drain magneto field effect transistor with high conductivity central drain	19980526 257/421
US 5751635 A	Read circuits for analog memory cells	19980512 365/185.19
US 5694356 A	High resolution analog storage EPROM and flash EPROM	19971202 365/185.03
US 5687115 A	Write circuits for analog memory	19971111 365/185.03

US 5650979 A	Semiconductor read-only VLSI memory	19970722 365/233.5
US 5638320 A	High resolution analog storage EPROM and flash EPROM	19970610 365/185.03
US 5540729 A	Movement powered medical pulse generator having a full-wave rectifier with dyna	19960730 607/35
US 5534848 A	Automotive fault tolerant serial communication	19960709 340/517
US 5436552 A	Clamping circuit for clamping a reference voltage at a predetermined level	19950725 323/313
US 5414663 A	VLSI memory with an improved sense amplifier with dummy bit lines for modeling	19950509 365/210
US 5374859 A	Low power dual power supply high resolution comparator	19941220 327/65
US 5365547 A	1X asynchronous data sampling clock for plus minus topology applications	19941115 375/259
US 5241497 A	VLSI memory with increased memory access speed, increased memory cell densi	19930831 365/185.16
US 5109163 A	Integrated power-on reset circuit	19920428 327/143
US 5013993 A	Thermally responsive battery charger	19910507 320/150
US 4908527 A	Hall-type transducing device	19900313 327/511
US 4877976 A	Cascade FET logic circuits	19891031 326/117
US 4857769 A	Threshold voltage fluctuation compensation circuit for FETS	19890815 327/541
US 4612629 A	Highly scalable dynamic RAM cell with self-signal amplification	19860916 365/185.08
US 4585955 A	Internally regulated power voltage circuit for MIS semiconductor integrated circuit	19860429 327/541
US 4449224 A	Dynamic merged load logic (MLL) and merged load memory (MLM)	19840515 377/79
US 4448400 A	Highly scalable dynamic RAM cell with self-signal amplification	19840515 365/185.03
US 4434479 A	Nonvolatile memory sensing system	19840228 365/210
US 4417325 A	Highly scaleable dynamic ram cell with self-signal amplification	19831122 365/185.08
US 4414503 A	Low voltage regulation circuit	19831108 323/315
US 4213142 A	Semiconductor device and method	19800715 257/400
US 4130890 A	Integrated DDC memory with bitwise erase	19781219 365/184
US 4071784 A	MOS input buffer with hysteresis	19780131 327/206
US 3989034 A	Apparatus and method for signaling fetal distress and uterine contraction monitor	19761102 600/511
US RE28905 E	Field effect transistor memory cell	19760713 365/190
US 3903431 A	Clocked dynamic inverter	19750902 326/88
US 3845324 A	DUAL VOLTAGE FET INVERTER CIRCUIT WITH TWO LEVEL BIASING	19741029 326/119
US 3794999 A	NOISE-FIGURE MEASURING CIRCUIT	19740226 342/168
US 3663835 A	FIELD EFFECT TRANSISTOR CIRCUIT	19720516 327/581
US 20020018362 A	Programmable circuit for DRAM, has latch circuit which applies threshold voltage t	20020214
<b>Results of search set L5: dominant logic.CLM.</b>		
US 20040230935 A1	Method and Apparatus for Creating Circuit Redundancy in Programmable Logic D	20041118 716/17
US 5778204 A	High-speed dominant mode bus for differential signals	19980707 710/305
US 5493657 A	High speed dominant mode bus for differential signals	19960220 710/305
US 5485458 A	Bus interconnect circuit including port control logic for a multiple node communicat	19960116 370/409
US 4055906 A	Automated interrogating apparatus	19771101 434/325